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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
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Application Number	10722218	Filing Date	2003-11-25	Docket Number (if applicable)	2003-0959 / 24061.149	Art Unit	2814
First Named Inventor	Shui-Ming Cheng et al.			Examiner Name	Cao, Phat X.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
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SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

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- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
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MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

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FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 081394

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (03/08)
Approved for use through 05/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Signature of Registered U.S. Patent Practitioner			
Signature	/Kelly Gehrke Lyle/	Date (YYYY-MM-DD)	2008-07-17
Name	Kelly Gehrke Lyle	Registration Number	62332

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REPLY UNDER 37 CFR §1.116
EXPEDITED PROCEDURE
ART GROUP 2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Shui-Ming Cheng, et al.	§	Confirmation No.: 6790
Serial No.: 10/722,218	§	Group Art Unit: 2814
Filed: November 25, 2003	§	Examiner: Cao, Phat X.
For: Semiconductor Device Having High Drive Current and Method of Manufacture Therefor	§	Attorney Docket No.: 2003-0959/ 24061.149

Commissioner for Patents
Mail Stop RCE
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE ACCOMPANYING RCE

This Amendment is being submitted concurrently with an RCE request. A one-month extension is believed necessary for consideration of this paper and the Commissioner is hereby authorized to charge the one-month extension fee to Haynes and Boone,LLP's Deposit Account No. 08-1394.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device, comprising:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein a first one of the NMOS and PMOS devices includes first source/drain regions recessed within the surface, wherein the first source/drain regions are disposed entirely below the surface of the substrate; and

wherein a second one of the NMOS and PMOS devices includes second source/drain regions at least partially extending above the surface.

2. (Original) The semiconductor device of claim 1 wherein:

a high-gate one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and having a first height over the surface; and

a low-gate one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and having a second height over the surface, wherein the first height is substantially greater than the second height.

3. (Original) The semiconductor device of claim 1 wherein:

a wide-spacer one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and first spacers on opposing sides of the first gate, the first spacers each extending from the first gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and second spacers on opposing sides of the second gate, the second spacers each extending from the second gate to a second width, wherein the first width is substantially greater than the second width.

4. (Original) The semiconductor device of claim 2 wherein:

a wide-spacer one of the NMOS and PMOS devices includes first spacers on opposing sides of an associated one of the first and second gates, the first spacers each extending from the associated gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes second spacers on opposing sides of an associated one of the first and second gates, the second spacers each extending from the associated gate to a second width, wherein the first width is substantially greater than the second width.

5. (Original) The semiconductor device of claim 1 wherein at least one set of the first and second source/drain regions comprises SiGe.

6. (Original) The semiconductor device of claim 1 wherein at least one set of the first and second source/drain regions comprises SiC.

7. (Original) The semiconductor device of claim 6 wherein at least one set of the first and second source/drain regions comprise SiGe.

8. (Original) The semiconductor device of claim 1 wherein the substrate has a <110> crystal orientation.

9. (Original) The semiconductor device of claim 1 wherein the substrate has a <100> crystal orientation.

10. (Original) The semiconductor device of claim 1 wherein the substrate is a silicon-on-insulator substrate.

11. (Original) The semiconductor device of claim 1 wherein the substrate is a bulk silicon substrate.

12. (Original) The semiconductor device of claim 1 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

13. (Original) The semiconductor device of claim 2 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

14. (Original) The semiconductor device of claim 3 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

15. (Original) The semiconductor device of claim 1 further comprising an etch stop layer located over the NMOS and PMOS devices and imparting a first stress in the first source/drain regions and a second stress in the second source/drain regions, wherein the first and second stresses are substantially different in magnitude.

16. (Currently Amended) A semiconductor device, comprising:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein a first one of the NMOS and PMOS devices includes:

first source/drain regions recessed within the substrate; and

a first gate interposing the first source/drain regions and having a first gate height over the surface, wherein the first source and drain regions are disposed entirely below an imaginary plane extending from the interface of the gate and the substrate; and

wherein a second one of the NMOS and PMOS devices includes:

second source/drain regions at least partially extending above the surface, and extending at least partially above the imaginary plane extending from the interface of the gate and the substrate; and

a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different.

17. (Original) The semiconductor device of claim 16 wherein:

a wide-spacer one of the NMOS and PMOS devices includes first spacers on opposing sides of an associated gate, the first spacers each extending from the associated gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes second spacers on opposing sides of an associated gate, the second spacers each extending from the associated gate to a second width, wherein the first width is substantially greater than the second width.

18. (Original) The semiconductor device of claim 16 wherein at least one set of the first and second source/drain regions comprises SiGe.

19. (Original) The semiconductor device of claim 16 wherein at least one set of the first and second source/drain regions comprises SiC.

20. (Original) The semiconductor device of claim 19 wherein at least one set of the first and second source/drain regions comprises SiGe.

21. (Original) The semiconductor device of claim 16 wherein the substrate has a <110> crystal orientation.

22. (Original) The semiconductor device of claim 16 wherein the substrate has a <100> crystal orientation.

23. (Original) The semiconductor device of claim 16 wherein the substrate is a silicon-on-insulator substrate.

24. (Original) The semiconductor device of claim 16 wherein the substrate is a bulk silicon substrate.

25. (Previously Presented) The semiconductor device of claim 16 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

26. (Previously Presented) The semiconductor device of claim 17 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

27. (Previously Presented) The semiconductor device of claim 16 further comprising an etch stop layer located over the NMOS and PMOS devices and contributing to the substantial

magnitude difference between the first stress in the first source/drain regions and the second stress in the second source/drain regions.

28. (Currently Amended) A semiconductor device, comprising:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein a first one of the NMOS and PMOS devices includes:

first source/drain regions recessed within the substrate, wherein a first contact coupled to the first source/drain region extends below the surface of the substrate;

a first gate interposing the first source/drain regions; and

first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and

wherein a second one of the NMOS and PMOS devices includes:

second source/drain regions at least partially extending above the surface;

a second gate interposing the second source/drain regions; and

second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different.

29. (Original) The semiconductor device of claim 28 wherein at least one set of the first and second source/drain regions comprises SiGe.

30. (Original) The semiconductor device of claim 28 wherein at least one set of the first and second source/drain regions comprises SiC.

31. (Original) The semiconductor device of claim 30 wherein at least one set of the first and second source/drain regions comprises SiGe.

32. (Original) The semiconductor device of claim 28 wherein the substrate has a <110> crystal orientation.

33. (Original) The semiconductor device of claim 28 wherein the substrate has a <100> crystal orientation.

34. (Original) The semiconductor device of claim 28 wherein the substrate is a silicon-on-insulator substrate.

35. (Original) The semiconductor device of claim 28 wherein the substrate is a bulk silicon substrate.

36. (Original) The semiconductor device of claim 28 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

37. (Previously Presented) The semiconductor device of claim 28 further comprising an etch stop layer located over the NMOS and PMOS devices and contributing to the substantial magnitude difference between the first stress in the first source/drain regions and the second stress in the second source/drain regions.

38. (Currently Amended) A semiconductor device, comprising:
an isolation region located in a substrate;
an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein a first one of the NMOS and PMOS devices includes first source/drain regions located at least partially within the substrate and comprising SiC; and

wherein a second one of the NMOS and PMOS devices includes second source/drain regions located at least partially within the substrate and comprising SiGe, wherein one of the first and second source/drain regions is disposed entirely within the substrate, and wherein one of first and second source/drain regions extends from the surface of the substrate.

39. (Original) The semiconductor device of claim 38 wherein the first source/drain regions are recessed within the surface and the second source/drain regions extend from the surface.

40. (Original) The semiconductor device of claim 38 wherein:

a high-gate one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and having a first height over the surface; and

a low-gate one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and having a second height over the surface, wherein the first height is substantially greater than the second height.

41. (Original) The semiconductor device of claim 38 wherein:

a wide-spacer one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and first spacers on opposing sides of the first gate, the first spacers each extending from the first gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes a second gate interposing associated second source/drain regions and second spacers on opposing sides of the second gate, the second spacers each extending from the second gate to a second width, wherein the first width is substantially greater than the second width.

42. (Original) The semiconductor device of claim 38 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

43. (Original) The semiconductor device of claim 38 further comprising an etch stop layer located over the NMOS and PMOS devices and imparting a first stress in the first source/drain regions and a second stress in the second source/drain regions, wherein the first and second stresses are substantially different in magnitude.

44. (Currently Amended) A method of manufacturing a semiconductor device, comprising:
forming an isolation region located in a substrate;
forming an NMOS device located partially over a surface of the substrate; and
forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
wherein a first one of the NMOS and PMOS devices includes first source/drain regions recessed within the surface, wherein the entire first source/drain region is recessed within the surface; and
wherein a second one of the NMOS and PMOS devices includes second source/drain regions at least partially extending above the surface.

45. (Original) The method of claim 44 wherein:
a high-gate one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and having a first height over the surface; and
a low-gate one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and having a second height over the surface, wherein the first height is substantially greater than the second height.

46. (Original) The method of claim 44 wherein:

a wide-spacer one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and first spacers on opposing sides of the first gate, the first spacers each extending from the first gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and second spacers on opposing sides of the second gate, the second spacers each extending from the second gate to a second width, wherein the first width is substantially greater than the second width.

47. (Currently Amended) An integrated circuit device, comprising:

a plurality of semiconductor devices each including:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein, in ones of the plurality of semiconductor devices, a first one of the NMOS and PMOS devices includes first source/drain regions entirely recessed within the surface; and

wherein, in ones of the plurality of semiconductor devices, a second one of the NMOS and PMOS devices includes second source/drain regions at least partially extending above the surface; and

a plurality of interconnects connecting ones of the plurality of semiconductor devices.

48. (Original) The integrated circuit device of claim 47 wherein, in each of the plurality of semiconductor devices having one of source/drain regions recessed within the surface and source drain regions extending from the surface:

a high-gate one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and having a first height over the surface; and

a low-gate one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and having a second height over the surface, wherein the first height is substantially greater than the second height.

49. (Original) The integrated circuit device of claim 47 wherein, in each of the plurality of semiconductor devices having one of source/drain regions recessed within the surface and source drain regions extending from the surface:

a wide-spacer one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and first spacers on opposing sides of the first gate, the first spacers each extending from the first gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and second spacers on opposing sides of the second gate, the second spacers each extending from the second gate to a second width, wherein the first width is substantially greater than the second width.

REMARKS

This Amendment is being submitted concurrently with a Request for Continued Examination (RCE). Claims 1, 16, 28, 38, 44 and 47 have been amended. Claims 1-49 are presently pending in the application. No new matter has been added by way of the foregoing amendment. Further and favorable consideration of the application is respectfully requested.

§ 102 Rejection of Claim 1

Claims 1, 11, and 44 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. App. No. 2005/0079660 to Murthy, et al. ("Murthy").

The Examiner argues that "one of ordinary skill in the art would have no difficulty to recognize that the bottom portions of the source/drain regions 46 N/P formed within the recesses 40 N/P shown in Fig. 3 are 'sunken area' that fall below the surface of the substrate 22." Advisory Action, pg. 2. Emphasis added. The Examiner continues "[f]urthermore, Murthy clearly states at paragraph [0031] that '...The source and drain regions 46P are formed by epitaxially growing pure germanium with the source and drain recesses 40P. The source and drain regions 46N are formed by growing pure germanium within the source and drain recesses 40N." Id.

Murthy figure referenced by the Examiner is reproduced below.

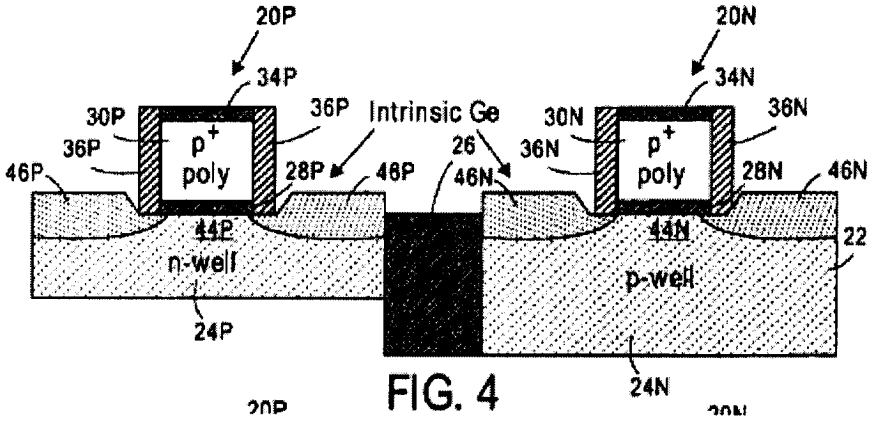

FIG. 4

Claim 1, as amended, requires "wherein a first one of the NMOS and PMOS devices includes first source/drain regions recessed within the surface, wherein the first source/drain regions are disposed entirely below the surface of the substrate." The Applicants respectfully submit that Murthy does not provide for a recessed source and drain region disposed entirely below the surface of the substrate. The Examiner indicates the bottom portion of the region provides the recessed source/drain, however, the claims as amended require the source/drain region to be entirely below the surface. As is illustrated in Fig. 1 of Murthy above, the source/drain regions 46 N/P extend above the substrate surface. Therefore, for at least this reason the claim is allowable.

Furthermore, even assuming the source/drain regions 46 N/P were considered recessed and disposed entirely in the substrate, which is clearly not the case, then the referenced Murthy embodiment does not provide for the second source/drain regions which extend above the substrate 22 as also provided in the claim.

Claim 44 as amended requires "wherein a first one of the NMOS and PMOS devices includes first source/drain regions recessed within the surface, wherein the entire first source/drain region is recessed within the surface; and wherein a second one of the NMOS and PMOS devices includes second source/drain regions at least partially extending above the surface." As described above with reference to claim 1, the cited portions of Murthy do not provide for the entire s/d region being recessed within the surface of a first s/d and a second s/d region partially extending above the surface. Therefore, claim 44 is allowable for at least these same reasons.

§103 Rejections

The Examiner has rejected claims 2-10, 12-43, and 45-49 under various combinations of art including Murthy.

In *KSR Int'l. Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1739 (2007), the Court stated that "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *Id.* at 1741 (emphasis added).

As the PTO recognizes in MPEP §2142:

> ... The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness...

In the present application, a *prima facie* case of obviousness does not exist for the claims as herein amended for the reasons set forth below.

1. The Examiner has not shown that all words in the claim have been considered

MPEP 2143.03 states that "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." Quoting *In re Wilson*, 424 F.2d 1382, 1385 (CCPA 1970). However, in the present matter, the Examiner has not shown that all words in the claim have been considered.

Independent claim 16 requires ...

> a first gate interposing the first source/drain regions and having a first gate height over the surface, wherein the first source and drain regions are disposed entirely below an imaginary plane extending from the interface of the gate and the substrate; and wherein a second one of the NMOS and PMOS devices includes: second source/drain regions at least partially extending above the surface, and extending at least partially above the imaginary plane extending from the interface of the gate and the substrate

As discussed above with reference to claim 1, the cited portions of Murthy do not provide for a source/drain region disposed entirely below an imaginary plane extending from the interface of the gate and the substrate, and a second source/drain region extending at least partially above this plane. Neither the Bohr reference nor the Dawson reference cited by the Examiner in the rejection of claim 16 cure this deficiency. Accordingly, Applicants respectfully request that the Examiner withdraw the § 103 rejection of claim 16, as amended, and the claims that depend therefrom for at least this reason.

Independent claim 28 requires,

> first source/drain regions recessed within the substrate, wherein a first contact coupled to the first source/drain region extends below the surface of the substrate; second source/drain regions at least partially extending above the surface;

Similarily to as discussed above with reference to claim 1, the cited portions of Murthy do not provide for a first contact coupled to the first source/drain region extends below the surface of the substrate. Though Fig. 4 does not explicitly include a contact, even assuming arguendo, a contact would be provided to regions 46 P/N, such a contact would not extend below the surface of the substrate as the 46 P/N region itself extends above the substrate 22. Neither the Bohr reference nor the Dawson reference cited by the Examiner in the rejection of claim 28 cure this deficiency. Accordingly, Applicants respectfully request that the Examiner withdraw the § 103 rejection of claim 28, as amended, and the claims that depend therefrom for at least this reason.

Independent claim 38, as amended requires:

> wherein one of the first and second source/drain regions is disposed entirely within the substrate, and wherein one of first and second source/drain regions extends from the surface of the substrate.

As described above with reference to claim 1, Murthy at least does not disclose a source/drain region entirely disposed within a substrate and a second source/drain region extending from the surface of the substrate. Yeo, referenced by the Examiner in the rejection of claim 38, fails to cure this deficiency. For at least this reason, claim 38 is allowable.

Dependent Claims

Dependent claims 2-15, 17-27, 29-37, 39-43, 45-46, and 48-49 depend from and further limit independent claims 1, 16, 28, 38, 44, and 47 and therefore are deemed to be patentable over the prior art.

Conclusion

It is believed that all claims are in condition for allowance. Favorable consideration and an early indication of allowability are respectfully requested.

Should the Examiner deem that an interview with Applicants' undersigned attorney would expedite consideration, the Examiner is invited to call the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

Kelly Gehrke Lyle
Registration No. 62,332

Dated: July 15, 08

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Document No.: R-203548.1

Certificate of Service

I hereby certify that this correspondence is being filed with the U.S. Patent and Trademark Office via EFS-Web on July 17, 2008.

Bonnie Boyle